IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A dual bank FIFO memory buffer, comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses;

a first write pointer associated with the first bank of memory elements, the first write pointer operable to allow received data to be written to the first bank of memory elements when a second write pointer is in a null state;

a second write pointer associated with the second bank of memory elements, the second write pointer operable to allow received data to be written to the second bank of memory elements when the first write pointer is in a null state;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined times by enabling the first and second write pointers at times dependent on received strobe signal preamble timing;

read control logic operable to read data stored in the first and second banks;

a first port connecting the dual bank FIFO memory buffer to a memory; and

a second port connecting the dual bank FIFO memory buffer to a memory controller.

2. (Previously Presented) The dual bank FIFO memory buffer of claim 1, wherein the memory data is provided by double data rate synchronous dynamic read only memory (DDR SDRAM) operatively connected to the buffer via the first port.

3. (Original) The dual bank FIFO memory buffer of claim 1, wherein the write control address logic is operable to determine an element within a bank of memory elements in which selected memory data is to be stored by evaluating rising and falling edges of a strobe signal.

4. (Original) The dual bank FIFO memory buffer of claim 3, wherein the determination of the element in which selected memory data is to be stored further comprises selection of sequential element addresses during sequential strobe cycles.

5. (Original) The dual bank FIFO memory buffer of claim 1, wherein the write control timing logic comprises a write pointer associated with each FIFO bank.

6. (Original) The dual bank FIFO memory buffer of claim 5, wherein each write pointer is operable to control write access to its associated FIFO bank.

7. (Original) The dual bank FIFO memory buffer of claim 6, wherein write access is granted via write pointer only during predetermined time periods when the read data is determined to be valid.

8. (Original) The dual bank FIFO memory buffer of claim 7, wherein determination that the read data is valid comprises determination that a programmed expected time delay after issuing a read request has occurred.

9. (Original) The dual bank FIFO memory buffer of claim 8, wherein the programmed expected time delay is determined independently for different units of memory.

10. (Previously Amended) A dual bank FIFO memory buffer, comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses, the selected addresses determined by evaluation of a strobe signal;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined time, the write control timing logic comprising a write

pointer associated with each FIFO bank and operable to control write access to the associated bank during periods when read data is determined to be valid;

read control logic operable to read data stored in the first and second banks;

a first port connecting the dual bank FIFO memory buffer to a memory; and

a second port connecting the dual bank FIFO memory buffer to a memory controller.

11. (Currently Amended) A memory controller, comprising:

a command signal output operable to issue a data read command;

a data input operable to receive read data from a memory; and

a dual-bank FIFO connected between the data input and the memory and operable to buffer the read data, the dual-bank FIFO further comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses;

a first write pointer associated with the first bank of memory elements, the first write pointer operable to allow received data to be written to the first bank of memory elements when a second write pointer is in a null state;

a second write pointer associated with the second bank of memory elements, the second write pointer operable to allow received data to be written to the second bank of memory elements when the first write pointer is in a null state;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined times by enabling the first and second write pointers at times dependent on received strobe signal preamble timing; and

read control logic operable to read data stored in the first and second banks.

12. (Original) The memory controller of claim 11, wherein the memory data is provided by double data rate synchronous dynamic read only memory (DDR SDRAM) operatively connected to the buffer.

13. (Original) The memory controller of claim 11, wherein the write control address logic is operable to determine an element within a bank of memory elements in which selected memory data is to be stored by evaluating rising and falling edges of a strobe signal.

14. (Original) The memory controller of claim 13, wherein the determination of the element in which selected memory data is to be stored further comprises selection of sequential element addresses during sequential strobe cycles.

15. (Original) The memory controller of claim 11, wherein the write control timing logic comprises a write pointer associated with each FIFO bank.

16. (Original) The memory controller of claim 15, wherein each write pointer is operable to control write access to its associated FIFO bank.

17. (Original) The memory controller of claim 16, wherein write access is granted via write pointer only during predetermined time periods when the read data is determined to be valid.

18. (Original) The memory controller of claim 17, wherein determination that the read data is valid comprises determination that a programmed expected time delay after issuing a read request has occurred.

19. (Original) The memory controller of claim 18, wherein the programmed expected time delay is determined independently for different units of memory.

20. (Currently Amended) A computerized information handling system, the system comprising:

a memory controller;

a memory;

a processor; and

a dual-bank FIFO connected between the memory and the memory controller and operable to buffer read data, the dual-bank FIFO further comprising:

a first bank of memory elements operable to buffer memory data;

a second bank of memory elements operable to buffer memory data;

write control address logic operable to store selected memory data in memory elements with selected addresses;

a first write pointer associated with the first bank of memory elements, the first write pointer operable to allow received data to be written to the first bank of memory elements when a second write pointer is in a null state;

a second write pointer associated with the second bank of memory elements, the second write pointer operable to allow received data to be written to the second bank of memory elements when the first write pointer is in a null state;

write control timing logic operable to selectively grant write access to the banks of memory elements at predetermined times by enabling the first and second write pointers at times dependent on received strobe signal preamble timing; and

read control logic operable to read data stored in the first and second banks.

21. (Original) The dual bank FIFO memory buffer of claim 1, wherein the memory data is provided by double data rate synchronous dynamic read only memory (DDR SDRAM) operatively connected to the buffer.

22. (Original) The dual bank FIFO memory buffer of claim 20, wherein the write control address logic is operable to determine an element within a bank of memory elements in which selected memory data is to be stored by evaluating rising and falling edges of a strobe signal.

23. (Original) The dual bank FIFO memory buffer of claim 22, wherein the determination of the element in which selected memory data is to be stored further comprises selection of sequential element addresses during sequential strobe cycles.

24. (Original) The dual bank FIFO memory buffer of claim 20, wherein the write control timing logic comprises a write pointer associated with each FIFO bank.

25. (Original) The dual bank FIFO memory buffer of claim 24, wherein each write pointer is operable to control write access to its associated FIFO bank.

26. (Original) The dual bank FIFO memory buffer of claim 25, wherein write access is granted via write pointer only during predetermined time periods when the read data is determined to be valid.

27. (Original) The dual bank FIFO memory buffer of claim 26, wherein determination that the read data is valid comprises determination that a programmed expected time delay after issuing a read request has occurred.

28. (Original) The dual bank FIFO memory buffer of claim 27, wherein the programmed expected time delay is determined independently for different units of memory.

29. (Previously Amended) A method of compensating for potential read loop delay timing-induced read errors, comprising:

selectively granting write access to a bank of FIFO buffer memory selected from a multi-bank FIFO of memory elements at determined time via write control timing logic, the write control timing logic comprising a write pointer associated with each FIFO bank and operable to control write access to the associated bank during periods when read data is determined to be valid, the multi-bank FIFO coupled between a memory and a memory controller.